

M5201AL/P/FP

GENERAL PURPOSE SWITCHING OPERATIONAL AMPLIFIER
(DUAL INPUT, SINGLE OUTPUT TYPE)

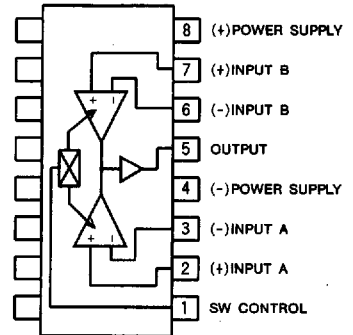
DESCRIPTION

The M5201A is a semiconductor integrated circuit designed for an operational amplifier with analog switching, dual A and B input, and a single output. The device comes in an 8-pin SIP, DIP or FP and contains input differential A and B circuits, single output circuit and operational amplifier switching circuit, and can be used as a conventional operational amplifier, activating on A or B input by externally setting the control pin level high or low. For a voltage follower condition where $G_v=0\text{dB}$, the device functions merely as an analog switch, but, for switching amplifier function, gain can be set independently for A and B input. The M5201A operational amplifier has basic characteristics similar to those of the M5218/M5R4558P and can be used in audio, video and musical instrument equipment.

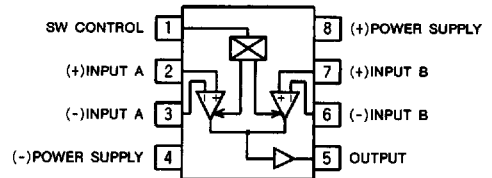
FEATURES

- Operational amplifier A and B input and gain can be set independently
- Applicable to both single and dual power supplies
- High gain, low distortion
 - $G_v=100\text{dB}$, $\text{THD} = 0.002\%$ (typ.)
- High slew rate, high f_r $\text{SR}=2.2\text{V}/\mu\text{s}$, $f_r = 7\text{MHz}$ (typ.)
- Low noise ($R_s=1\text{k}\Omega$) FLAT..... $V_{NI} = 2\mu\text{Vrms}$ (typ.)
- Low switching shock noise
- High load current, high power dissipation
 - $I_{LP} = \pm 50\text{mA}$, $P_d = 800\text{mW}$ (SIP)
 - $P_d = 625\text{mW}$ (DIP)
 - $P_d = 440\text{mW}$ (FP)

PIN CONFIGURATION (TOP VIEW)



Outline 8P5(AL)



Outline 8P4 (AP)
8P2S-A(AFP)

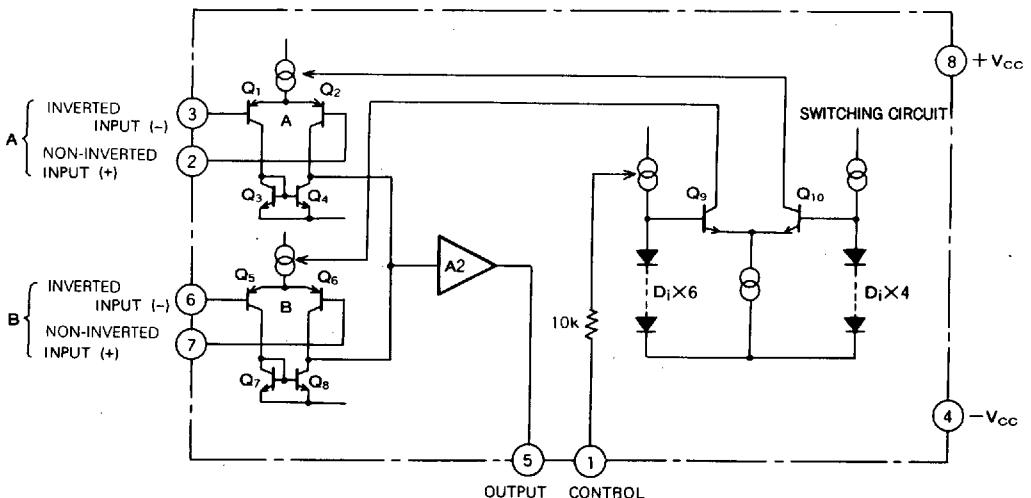
RECOMMENDED OPERATING CONDITION

Supply voltage range..... $\pm 2.5 \sim \pm 16\text{V}$
Rated supply voltage..... $\pm 15\text{V}$

APPLICATION

Component audio equipment, VCR, Tape recorder unit, etc.

EQUIVALENT CIRCUIT



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ABSOLUTE MAXIMUM RATINGS

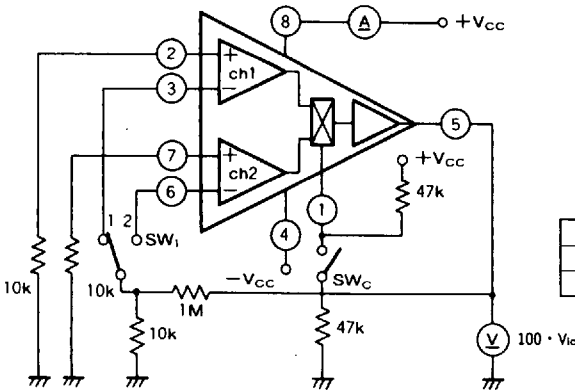
Symbol	Parameter	Ratings	Unit
V _{cc}	Supply voltage	±18 (36)	V
V _{id}	Differential input voltage	±30	V
V _{ic}	Common phase input voltage	±15	V
I _{LP}	Load current	±50	mA
P _d	Power dissipation	800 (SIP)/625 (DIP)/440 (FP)	mW
T _{opr}	Operating temperature	-20~75	°C
T _{stg}	Storage temperature	-55~125	°C

ELECTRICAL CHARACTERISTICS (T_a=25°C, V_{cc}=±15V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I _{cc}	Circuit current	V _{in} SW ON		2.3	6.0	mA
		SW OFF		2.1	6.0	
V _{io}	Input offset voltage	R _s =10kΩ		0.8	6.0	mV
I _b	Input bias current			80	500	nA
G _{vo}	Open loop voltage gain	R _L =2kΩ		100		dB
V _{om}	Maximum output voltage	R _L ≥10kΩ	±12	±14		V
THD	Total harmonic distortion	f=1kHz, V _o =5Vrms, G _v =20dB		0.002		%
SVR	Supply voltage rejection ratio			20	150	μV/V
C·S	Channel separation	f=1kHz		82		dB
f _r	Gain bandwidth product	G _v =0dB		7		MHz
SR	Slew rate	G _v =0dB, R _L =2kΩ//100pF		2.2		V/μs
V _{NI}	Input referred noise voltage	R _s =1kΩ, BW=10Hz~30kHz, Flat		2.0		μVrms

TEST CIRCUIT

(1) I_{cc}, V_{io}, SVR



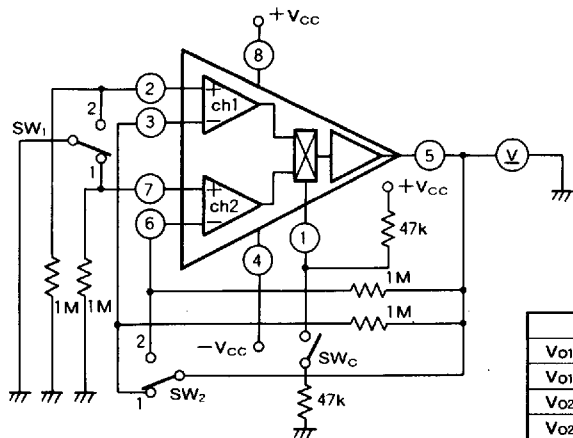
	SW _C	SW _I	Select ch
I _{cc1} , V _{io1} , SVR ₁	OFF	1	ch1
I _{cc2} , V _{io2} , SVR ₂	ON	2	ch2

Unit Resistance : Ω
capacitance : F

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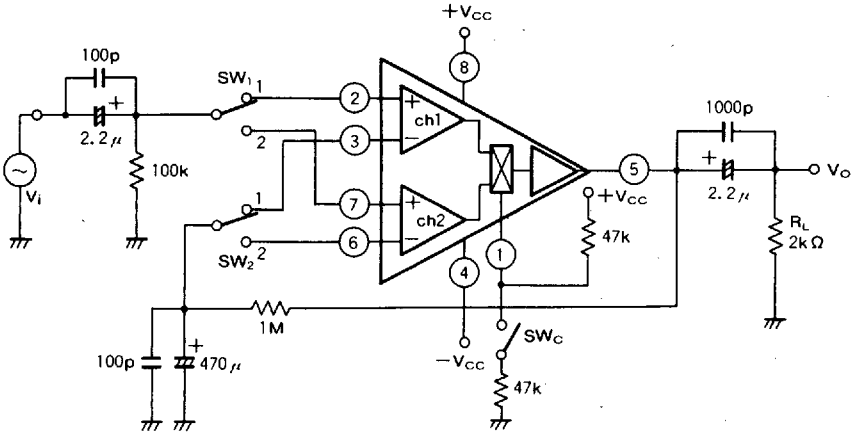
(2) I_b, I_o



$I_b^+ = V_{o1} / 1\text{M}\Omega$
 $I_b^- = V_{o2} / 1\text{M}\Omega$
 $I_{io} = |I_b^+ - I_b^-|$

	SWc	SW1	SW2	Select ch
V _{o1}	OFF	1	1	ch1
V _{o1}	OFF	2	2	ch1
V _{o2}	ON	2	2	ch2
V _{o2}	ON	1	1	ch2

(3) f_t, G_v



Unit Resistance : Ω
Capacitance : F

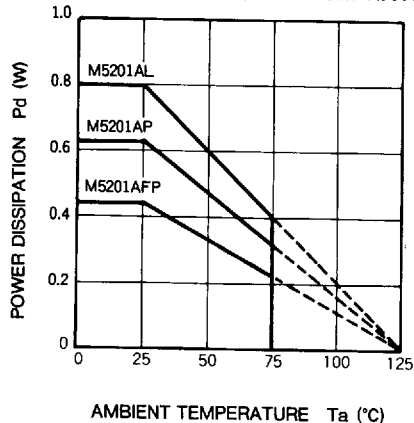
	SWc	SW1	SW2	Select ch
f_t, G_{v1}	OFF	1	1	ch1
f_t, G_{v2}	ON	2	2	ch2

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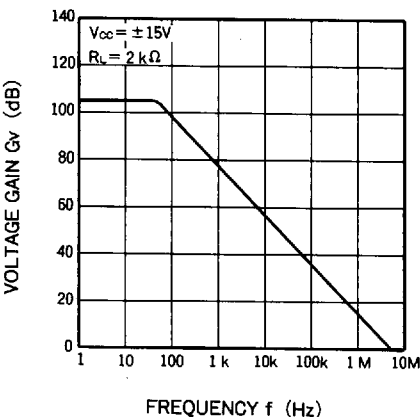
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TYPICAL CHARACTERISTICS

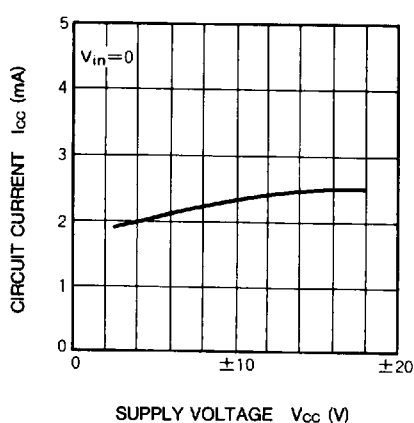
THERMAL DERATING (MAXIMUM RATING)



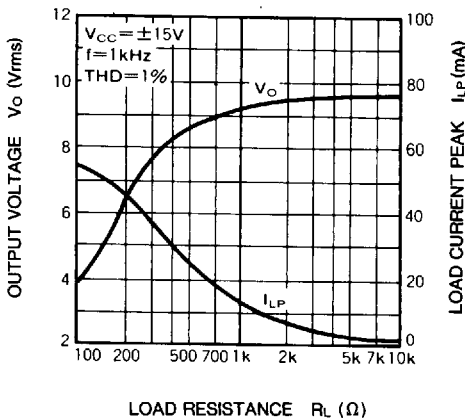
VOLTAGE GAIN VS. FREQUENCY RESPONSE



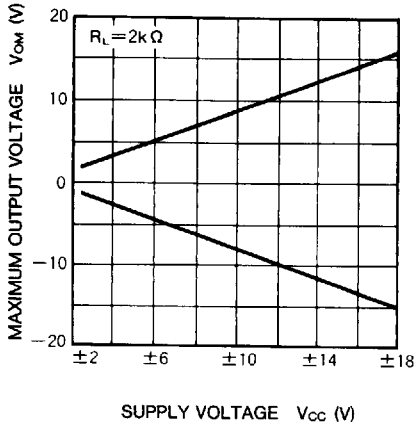
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



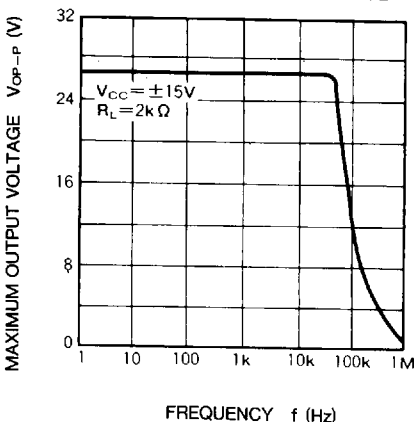
OUTPUT VOLTAGE/LOAD CURRENT PEAK VS. LOAD RESISTANCE



MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE

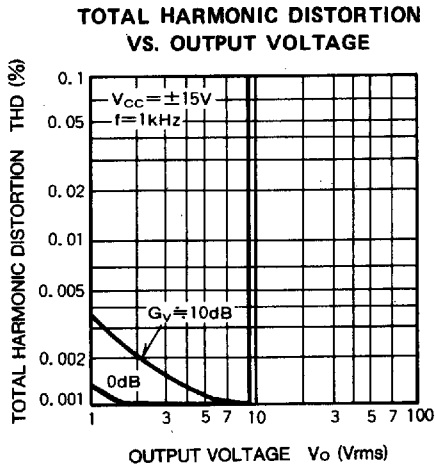
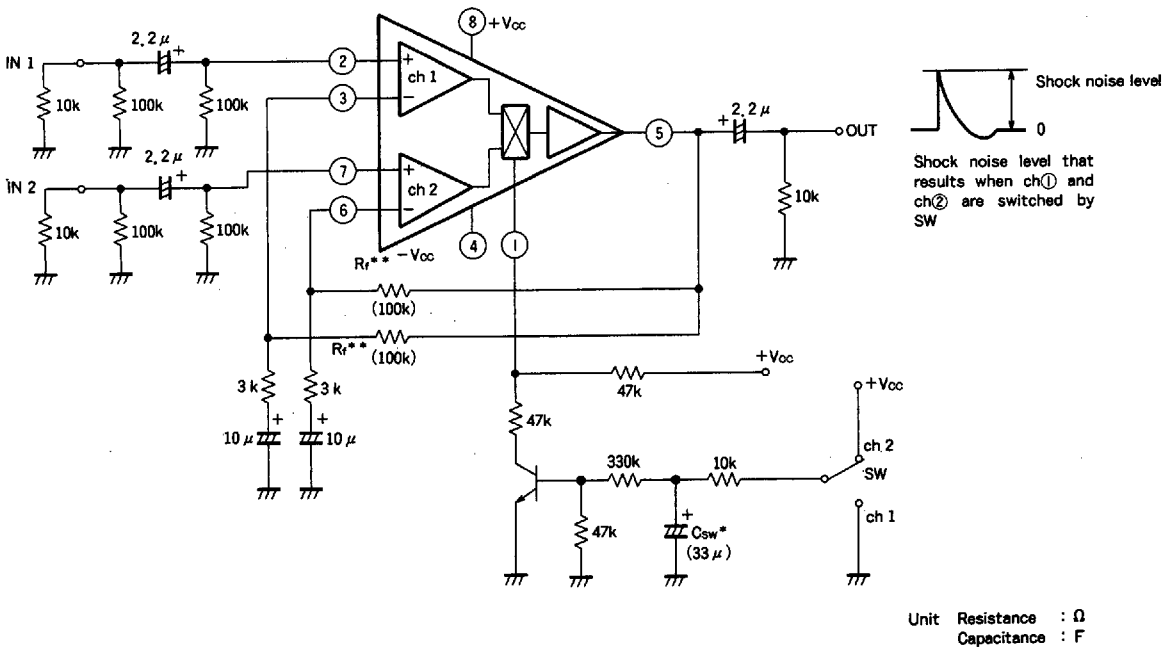


MAXIMUM OUTPUT VOLTAGE VS. FREQUENCY RESPONSE



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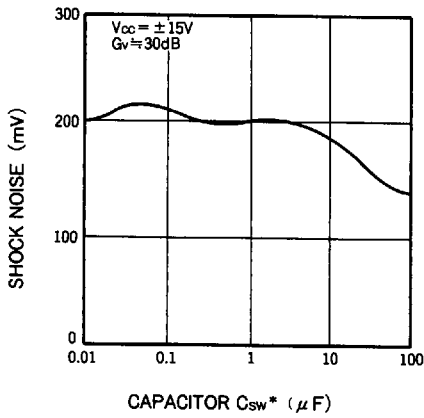
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**SHOCK NOISE MEASUREMENT****TEST CIRCUIT**

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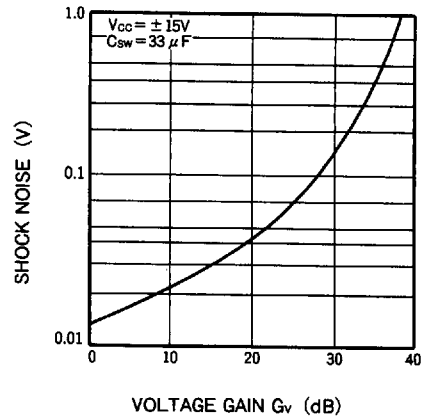
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SHOCK NOISE VS. CAPACITOR C_{sw}



* Characteristics of shock noise with respect to change of C_{sw}

SHOCK NOISE VS. VOLTAGE GAIN

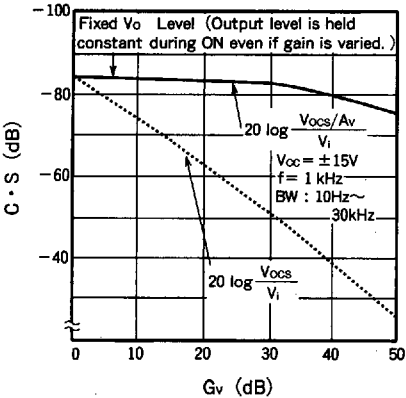


* * Characteristics of shock noise with respect to voltage gain varied by R_1 .

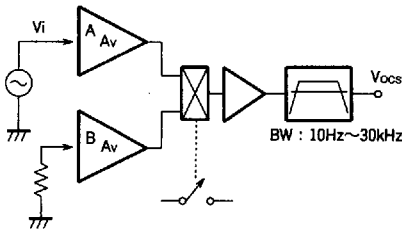
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CHANNEL SEPARATION CHARACTERISTICS



(A : OFF/B : IN ON MODE)



$$C \cdot S = 20 \log \left[\frac{\text{INPUT LEAK LEVEL}}{\text{SIGNAL LEVEL}} \right] \text{ (dB)}$$
$$= 20 \log \frac{V_{ocs}/A_v}{V_i} \text{ (dB)}$$

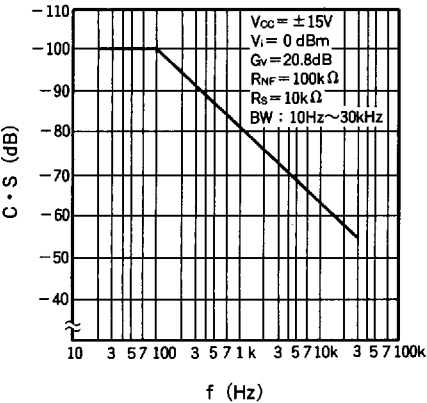
Channel separation is defined as ratio of leak signal (scaled on assumption it is present in input) to input signal.

$$\left(20 \log \frac{V_{ocs}/A_v}{V_i} \right)$$

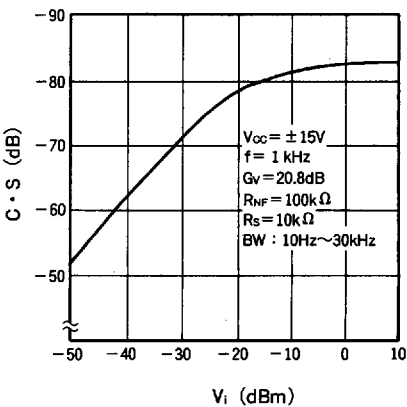
However, as indicated by above dashed line, if gain (A_v) is not scaled channel separation appears to deteriorate as much as amplified amount.

$$\left(20 \log \frac{V_{ocs}}{V_i} \right)$$

CHANNEL SEPARATION CHARACTERISTICS



CHANNEL SEPARATION CHARACTERISTICS

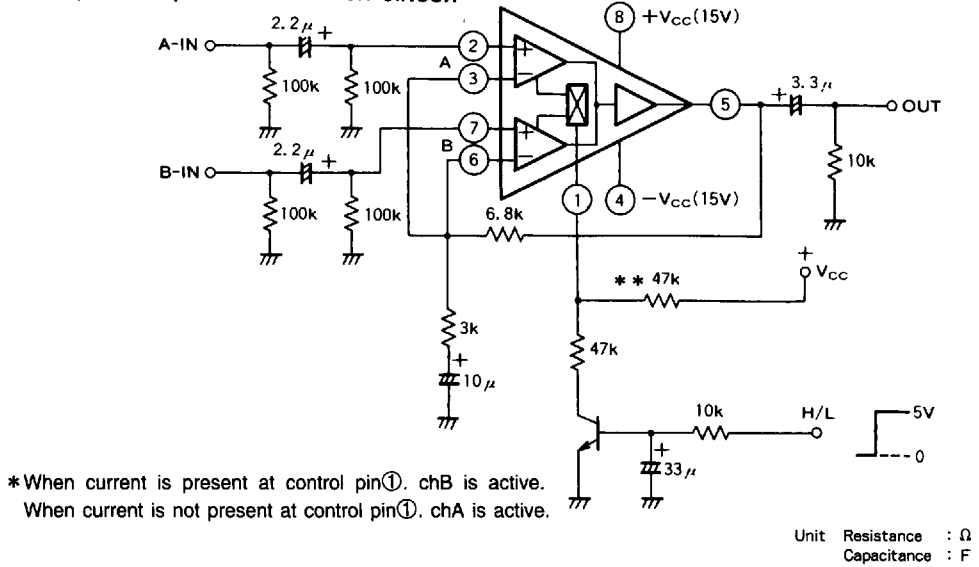


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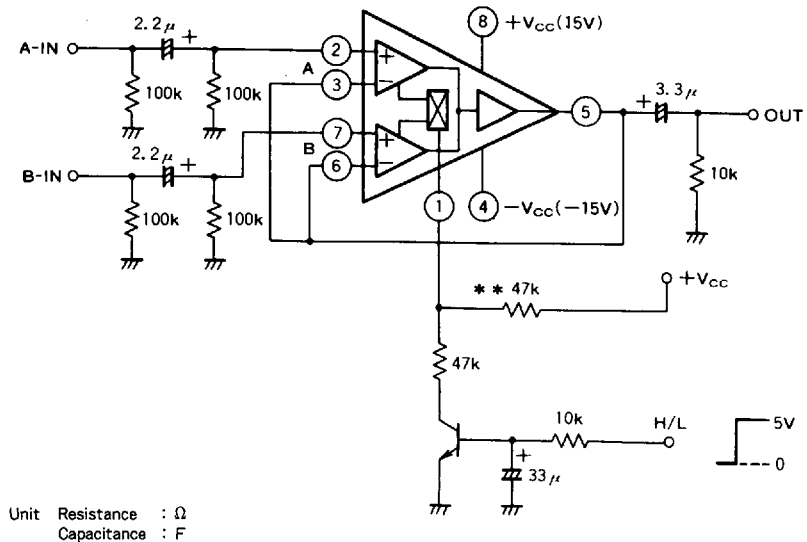
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APPLICATION EXAMPLE

(1) FLAT AMPLIFIER ($G_v \approx 10\text{dB}$) + ANALOG SWITCH CIRCUIT



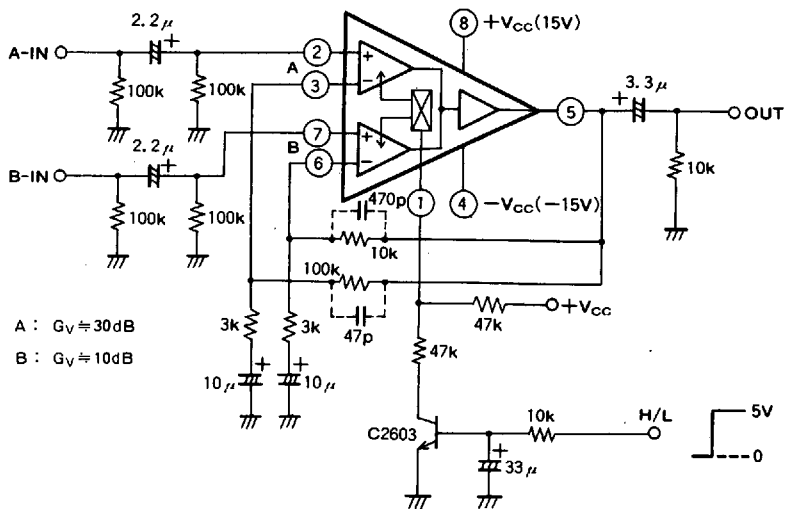
(2) ANALOG SWITCH CIRCUIT ($G_v = 0\text{dB}$, VOLTAGE FOLLOWER AMPLIFIER)



Resistor indicated by ** is a pull-up resistor to prevent switching pin ① from being activated by leak current from an external circuit.(i.e.TR).

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*When current is present at control pin①, chB is active.
When current is not present at control pin①, chA is active.

Unit Resistance : Ω
Capacitance : F

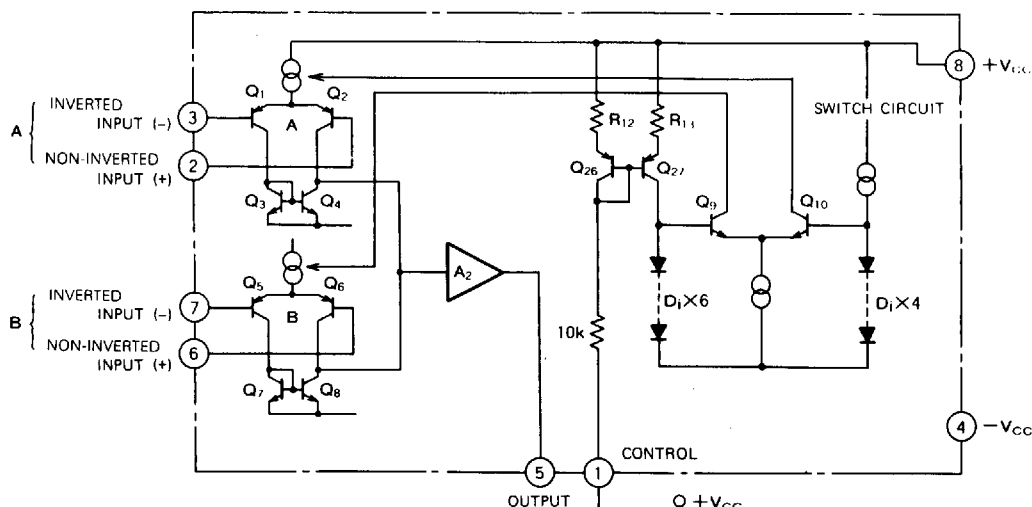
DESCRIPTION OF PIN

Pin No.	Name	Function
①	SW control	A/B channel select pin. By pulling current out from this pin, switching action is available.
②	(+) input A	Channel A op-amp (+) input pin
③	(-) input A	Channel A op-amp (-) input pin
④	(-) power supply	Negative power supply pin
⑤	Output	Output pin
⑥	(-) input B	Channel B op-amp (-) input pin
⑦	(+) input B	Channel B op-amp (+) input pin
⑧	(+) power supply	Positive power supply pin

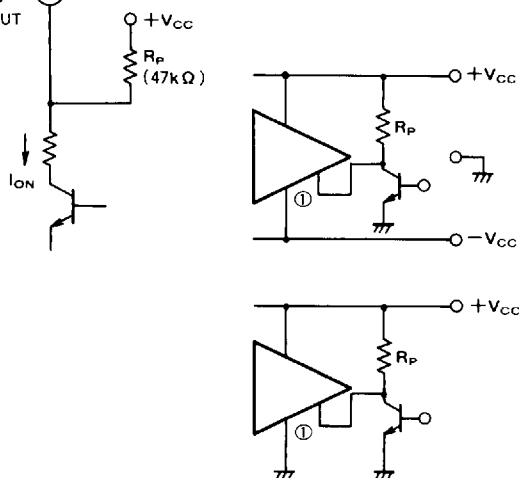
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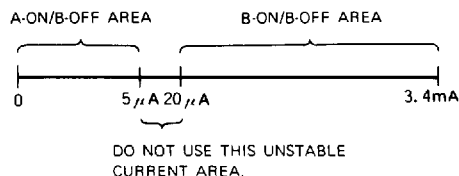
SWITCHING MECHANISM



As shown in above figure, the M5201A transfers switching signals by externally feeding current to V_F on Q_{26} side of current mirror transistor circuit (which consists of transistors Q_{26} and Q_{27}). That is, when no current is fed to pin ①, Q_{10} is turned on by four diodes connected to Q_{10} to activate channel A amplifier. When current is fed to pin ①, collector current of Q_9 flows to turn on six diodes connected to Q_9 and channel B is activated. Thus, applying or removing current to/from pin ① switches an active channel. Therefore, M5203A can arbitrarily control drive method regardless of power supply type (single or dual). It is recommended that a pull-up resistor R_P be connected to pin ① to reduce current sensitivity of transistor Q_{26} since very little current can turn on V_F .



PIN (1) TURN-ON CURRENT WHEN A PULL-UP RESISTOR R_P IS CONNECTED I_{ON} ($R_P = 47k\Omega$)



The diagram shows a 2SC2603 transistor inverter circuit. The input section has two options: IN 1 with a 100k resistor and IN 2 with a 2.2μF capacitor. The base is biased with a 47k resistor and a 0.0022μF capacitor. The output section has three options: OUT with a 10k resistor, H/L with a 47pF capacitor, and a 33μF capacitor. The circuit is powered by V_{CC} and GND. A central box indicates the circuit is applicable for SIP and DIP packages.